A Composite Multi-Layer design of GaN HEMT based PA for Compact Radar Applications

Priscilla Vasanthi A[1], Abhijat Khokar[2] & Ashwini U[3]
Microwave Components, Central- D&E,
Bharat Electronics, Bangalore
priscillavasanthia@bel.co.in

Abstract: ***This work aims at tactfully applying the Multi-layered PCB design approach to an S-Band Power Amplifier, thus providing for a compact yet viable solution to the present day Active Phased Array based Transmit-Receive (T/R) Modules. The paper takes one through the challenges faced by the authors during the course of migration from a Conventional 2- layer PCB approach to the one based on Multi-layered (ML) architecture. The novelty lies in successfully translating the Power Amplifier design that was hitherto realized on 2-layer stack up onto a multi-layer structure with minimum possible changes to the matching pattern.***

Keywords: GaN, HEMT, Power Amplifier, Multi – layer, Active Phased Array Radar (APAR), Transmit-Receive (T/R) module.

I. Introduction

Active phased arrays have emerged to be the predominant propositions for the modern day radar systems [1]. Active arrays use Transmit-Receive (T/R) modules mounted directly at each of their radiating elements (antenna) to provide the last stage of amplification for transmitted signals, the first stage of amplification for received signals, and provide both amplitude and phase control at each radiating element. An active phased array uses a special type of solid state transmitter module. The arrangement applied to most active phased arrays is shown in Figure 1.

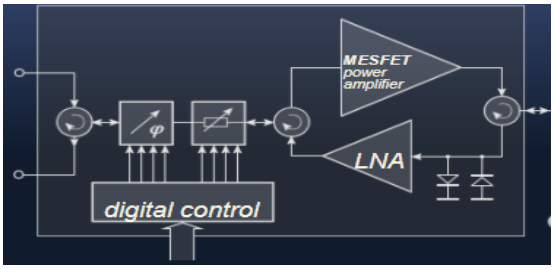

Figure 1. 2 – A typical T/R Module

In this way active array ensures a great degree of redundancy in case of failure of elements (graceful degradation). Also, for the same radiated power, active phased array systems have been found to be significantly efficient, smaller and lighter than the conventional passive array systems [1]. The whole concept of active phased array is critically dependent on the compactness in terms of size and weight, low power consumption and high reliability of the T/R modules. This compels us to look for and try out a different tack in designing them. One such area is to migrate from the conventional 2-layer PCB approach to a Multi-layer (ML) PCB architecture. Adoption of this architecture brings along merits related to reduction in size and wiring complexity (interconnections between PCBs in case of 2-layer design), as many functionalities can be built into a single PCB.

II. Problem Definition & Approach

This work showcases the application of ML design methodology to S-Band Power Amplifier (PA); a pivotal element in any T/R module. The S-Band PA was initially realized and proven on a 2-layer RF Substrate using discrete GaN on SiC based HEMT to generate >100W of power. The design was to be incorporated into a T/R module with restraints on the overall height of the module. This posed a hindrance to having a stack up of multiple two-layered PCBs in the design. Due to this constraint, the transistor along with its associated matching circuits were required to be realized on a composite 8-layer PCB. The ML PCB consisted of the same 2-layer RF PCB backed by 6 layers of FR4. The first layer consisted of the matching pattern and all other layers were dedicated to ground. Figures 2 and 3 below gives a glimpse of the PCB stack ups in case of 2- layer & the ML architectures. As is evident from the two figures, PCB thickness in case of a 2-Layer structure, the PCB thickness is 0.578mm whereas in case of a ML architecture it is 1.508mm. Clearly, a 3 fold increase in PCB thickness is observed that is indicative of the diversity of the conditions in the PA vicinity in either cases.

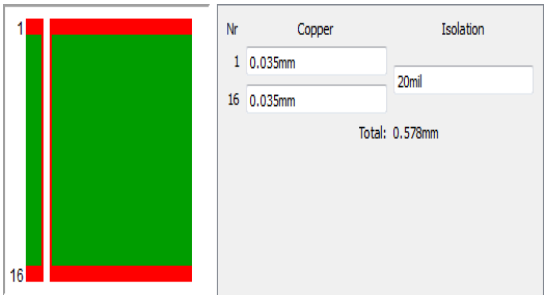

Figure 2. 2 – Layer PCB stack up

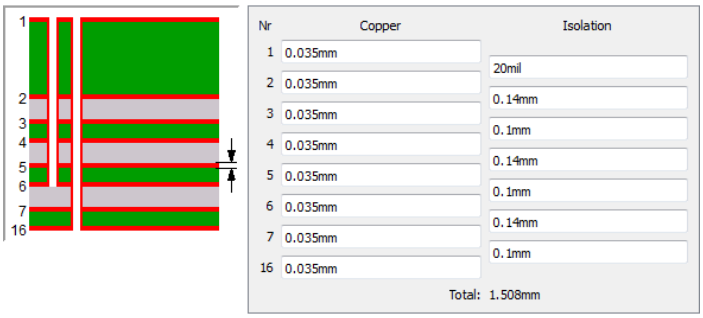

Figure 3. Multi- Layer PCB stack up

Also deducible from the above figures is the fact that in case of a 2- layer PCB there are only through vias that are predominantly for grounding. Whereas there are two types of vias in a ML architecture, one type that are through vias for grounding and the other type are from layers 1-6 and are blind from the bottom. They serve as connections to the power planes built on layer 6. Also layers 2-6 in the ML PCB is dedicated to ground in the PA vicinity & id free from routing.

III. Challenges in Redesigning

A lot of experimentation was carried out to realize the PA on ML PCB. Method of Moments (MoM) based Electromagnetic (EM) Simulation was carried out for the new stack up. Retaining the same 2-layer pattern, initial simulation results for ML PCB were not in good sync with the 2-layer design. It showed major impedance mismatches on input & output of the transistor. Figure 4 and 5 below are declarative of the same.

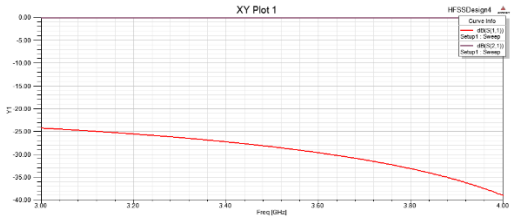

Figure 4. EM Simulation resultsof PA on 2 – Layer PCB

The reason for this varied results was the change in ground reference for micro-strip based matching pattern. Ground was immediate to the pattern on layer 1 as in case of 2 – Layer PCB but it was not so in case of the ML structure.

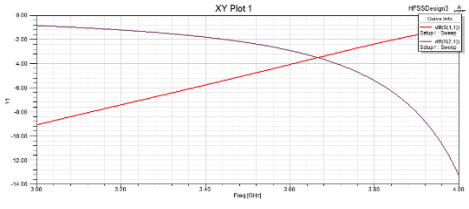

Figure 5. EM Simulation results of PA on Multi – Layer PCB

To solve this, the entire matching pattern of the transistor had to be worked upon as per the new ground reference. This resulted in an increased pattern size that violates the purpose of adopting ML PCB. After extensive research, provisioning for a number of blind-via holes (for better grounding) under the transistor matching pattern was thought could remedy this issue. As a consequence of a lot of trial and error in this direction, vias of size 1.2mm spaced 1.8mm were purveyed under the matching pattern as is shown in Figure 6.

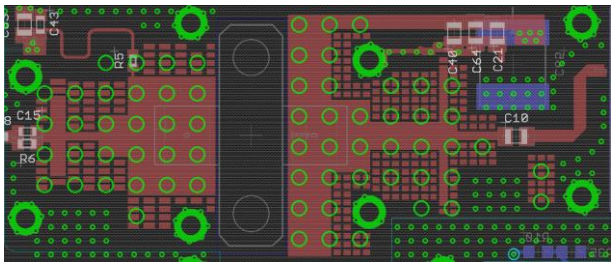

Figure 6. PA matching pattern with blind vias under

The vias provisioned were blind from top, i.e., they passed through layers 2-8. After this exercise, the input & output impedances of the transistor were matching with those observed on the 2-layer architecture. Figure 7 shows the iterated stack up that shows an extra via definition from layers 2-8. This method proved rewarding, as no major changes in the matching pattern were required. Figure 8 shows the simulated result of the matching pattern with blind vias under the pattern. It shows close resemblance to the impedances observed on the 2 – layer design.

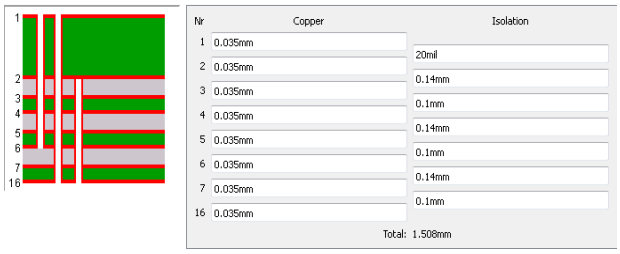

Figure 7. Revised Multi- Layer PCB stack up for the PA

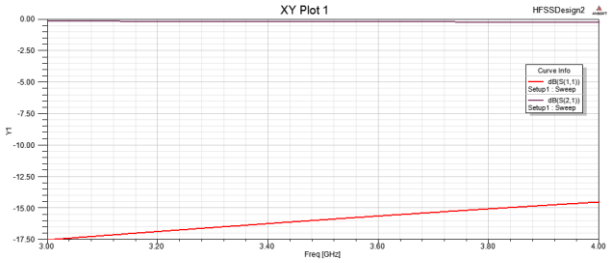

Figure 8. EM Simulation results of PA on ML PCB with blind vias under

IV. Fabrication & Performance Evaluation

The final ML PCB with the above features was fabricated. Also, “Edge-plating” was called for on all the exposed edges to further enhance the ground continuity between layers. Figure 9a &9b show the fabricated PCB. One could not distinguish between the 2 – Layer & ML PCBs from the top side as the pattern on both is the same. But from Figure 9b imprints of the 2-8 Layer vias are visible. Also evident from the figures is the edge plating that was called on all exposed edges of the PCB. The test results of the ML PCB showed similarity in performance with the 2-layer version of the same design in terms of critical parameters such as RF Output Power (>100W) and Harmonics (better than 30dBc).

Figure 10 shows the basic set-up that has been used for testing the Device under test (DUT). The test conditions for both the PCBs were alike and are as follows: Bias Sequencing of the PA was taken care of as PA being GaN based has special biasing & sequencing requirements. Also, Gate Pulsing mechanism was adopted for the PA where the gate bias voltage is switched alternately between normal bias and pinch-off in sync with the

Transmit/ Receive (TR) pulse. This pulsing technique has the advantage of easier circuit implementation because of the low current and voltage switching requirement. In the present work, it is implemented using a dual supply SPST switch, along with potential divider network incorporating "potentiometer", in order to facilitate finer adjustments in Gate bias voltage. All these functionalities were built onto a dedicated "Bias Sequencing & Gate Pulsing Card".

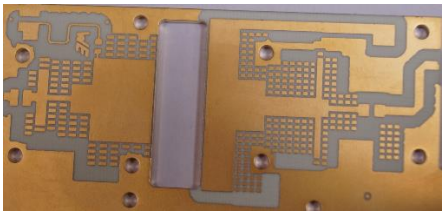

Figure 9a. Fabricated Multi- Layer PA PCB - Top side

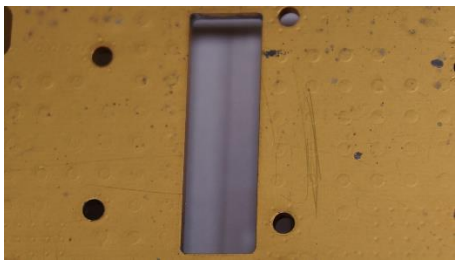

Figure 9b. Fabricated Multi- Layer PA PCB - Bottom side

The operating Drain Voltage reaching the device was 50V and the Gate Bias observed was -3V for the DUT, which was set by adjusting the potentiometer R_B. The DUT was tested for at 25, 50 and 100usec pulse widths and duties of 1 & 5% using the "Bias Sequencing & Gate Pulsing Card".

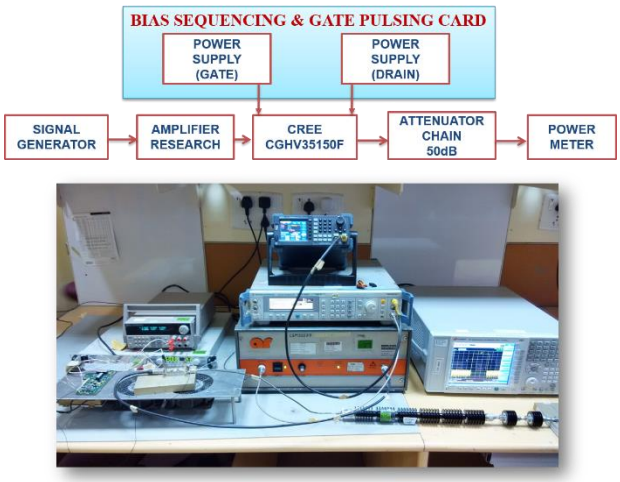

Figure 10. Experimental Set-up

Table 1 below shows a comparison in RF Power output from the two PCB variants with 51dBm being the targeted Output Power from the device whereas table 2 showcases the comparison between the harmonics generated, both tested at a Pulse width of 100usec & 1% duty.

	2- Layer		Multi - Layer	
Freq (GHz)	**O/P Power (dBm)**	**Droop (dB)**	**O/P Power (dBm)**	**Droop (dB)**
3.1	53.59	0.65	52	0.8
3.2	53.16	0.65	52.56	0.8
3.3	52.84	0.6	52.56	0.7
3.4	52.56	0.6	52.33	0.67
3.5	52.1	0.5	51.7	0.57

Table 1. Comparison of RF O/P Power

	2 – Layer – Harm (dBc)			ML – Harm (dBc)		
Freq (GHz)	**2^{nd} Harm**	**3^{rd} Harm**	**4^{th} Harm**	**2^{nd} Harm**	**3^{rd} Harm**	**4^{th} Harm**
3.1	39.4	55.2	32.2	37.36	63.46	44.66
3.2	36.6	47	35	46.4	56.5	57.2
3.3	37	39.7	41.7	51.27	37.37	70.87
3.4	34.6	31.4	46.6	52.03	35.63	68.03
3.5	35.1	30.4	52.4	46.62	51.52	60.22

Table 2. Comparison of Harmonic Performance

V. Conclusion

Power Amplifier is a solid state device that provides the last stage of amplification in the transmit chain of a T/R module. T/R module being the heart of any Active Phased Array Radar System, by virtue needs to be not only efficient but also miniaturized in size and so must be the PA inside. In this direction, a compact yet worthwhile solution to the Power Amplifier design using ML architecture has been presented. The authors have tried to uncover the fundamental differences in realizing an unmatched device in 2 – Layer and Multi – Layer architectures. The technique of providing blind vias under the matching pattern and "edge plating of the PCB" for better grounding is a simple and generic solution that can be applied to any unmatched device in an attempt to translate its design from a conventional 2 – Layer approach to a ML environment. Test results of the so realized ML PCB has shown close concurrence with its 2 – Layer counterpart.

Acknowledgement

We would like to acknowledge Mr. Naresh Kumar S, AGM, Microwave Components, C-D&E, BEL for his guidance, suggestions and constant encouragement.

.

References

[1] "T/R Module Technology", DRDO, Vol. 9 No.3 June 2001

[2] http://www.radartutorial.eu/.transmitters

[3] CREE Datasheet, CGHV35150F, www.wolfspeed.com.

Author's Bio Data

Priscilla Vasanthi A received her B.Tech. in Electronics and Communication Engineering from Jawaharlal Nehru Technological University in Hyderabad, India, and her M.E. in Microwave & Radar Engineering from Osmania University in Hyderabad, India. She joined Bharat Electronics in 2014 as a Deputy Engineer and has since been involved in developing Transmit-Receive Modules for Radar Systems.

Abhijat Khokhar completed his B.Tech in 2013 from JSS Academy of Technical Education NOIDA, India in Electronics and Communication. He received his M.Tech degree from GGSIP University Delhi in 2015 after that he worked as SRA in DRDO sponsored project for 8 months. Currently he is working in Bharat Electronics Limited as Deputy Engineer since April 2016 and his current work is on Transmit-Receive Modules for Radar Systems.

Ashwini U received her B.E. in Electronics and Communication Engineering from M.S.Ramaiah Institute of Technology, Bangalore, India. She joined Bharat Electronics in 2002 and is currently working as Manager in Central D&E -Microwave Components Group. She has been involved in developing RF power amplifiers for Communication Systems and Transmit-Receive Modules for Radar Systems.